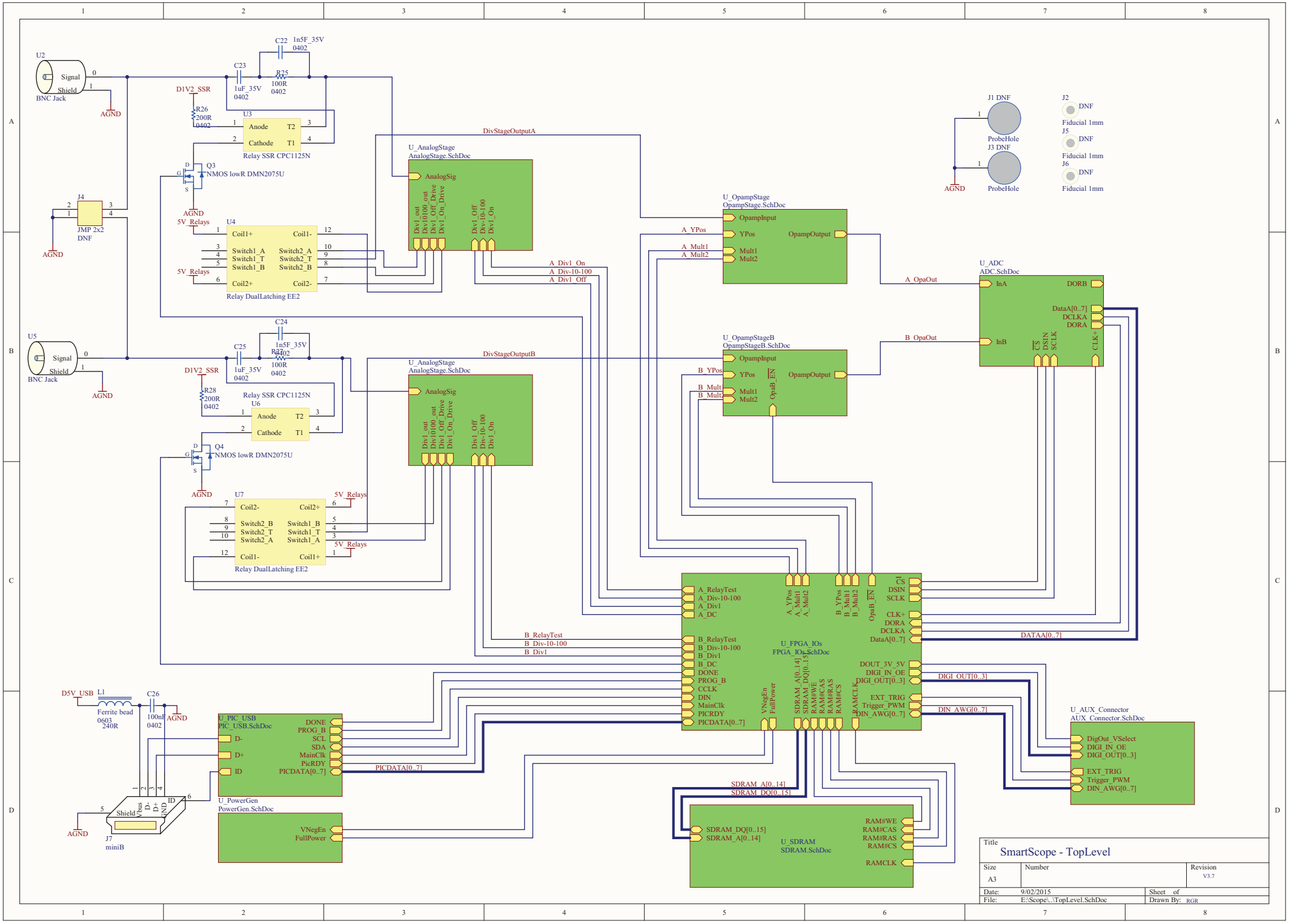
SmartScope

Schematics

Dec rev 1.1

Contents


U2
Signal
Shield
BNC Jack
AGND
C22 1n5F_35V 0402
C23 1uF_35V 0402
R25 100R 0402
D1V2_SSR
R26 200R 0402
U3
Anode T2
Cathode T1
Relay SSR CPC1125N
Q3 NMOS lowR DMN2075U
J4
JMP 2x2 DNF
5V_Relays
U4
Coil1+ Coil1-
Switch1_A Switch2_A
Switch1_T Switch2_T
Switch1_B Switch2_B
Coil2+ Coil2-
Relay DualLatching EE2
U_AnalogStage
AnalogStage.SchDoc
AnalogSig
Div1_out
Div10100_out
Div1_Off_Drive
Div1_On_Drive
Div1_Off
Div-10-100
Div1_On
DivStageOutputA
A_Div1_On
A_Div-10-100
A_Div1_Off
U_OpampStage
OpampStage.SchDoc
OpampInput
YPos
OpampOutput
Mult1
Mult2
A_YPos
A_Mult1
A_Mult2
A_OpaOut
U_ADC
ADC.SchDoc
InA
DORB
DataA[0..7]
DCLKA
DORA
InB
CS
DSIN
SCLK
CLK+
J1 DNF
J3 DNF
ProbeHole
J2 DNF Fiducial 1mm
J5 DNF Fiducial 1mm
J6 DNF Fiducial 1mm
U5
C24
C25 1uF_35V 0402
R27 100R 0402
R28 200R 0402
U6
U7
Q4 NMOS lowR DMN2075U
DivStageOutputB
B_YPos
B_Mult1
B_Mult2
OpaB_EN
B_OpaOut
B_RelayTest
B_Div-10-100
B_Div1
U_FPGA_IOs
FPGA_IOs.SchDoc
A_RelayTest
A_Div-10-100
A_Div1
A_DC
B_DC
DONE
PROG_B
CCLK
DIN
MainClk
PICRDY
PICDATA[0..7]
VNegEn
FullPower
SDRAM_A[0..14]
SDRAM_DQ[0..15]
RAM#WE
RAM#CAS
RAM#RAS
RAM#CS
RAMCLK
DOUT_3V_5V
DIGI_IN_OE
DIGI_OUT[0..3]
EXT_TRIG
Trigger_PWM
DIN_AWG[0..7]
DATAA[0..7]
D5V_USB
L1 Ferrite bead 0603 240R
C26 100nF 0402
U_PIC_USB
PIC_USB.SchDoc
D-
D+
ID
DONE
PROG_B
SCL
SDA
MainClk
PicRDY
PICDATA[0..7]
J7 miniB
Shield
Vbus
D-
D+
GND
U_PowerGen
PowerGen.SchDoc
U_SDRAM
SDRAM.SchDoc
U_AUX_Connector
AUX_Connector.SchDoc
DigOut_VSelect
DIGI_IN_OE
DIGI_OUT[0..3]
EXT_TRIG
Trigger_PWM
DIN_AWG[0..7]
Title
SmartScope - TopLevel
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Number
Revision
V3.7
Date: 9/02/2015
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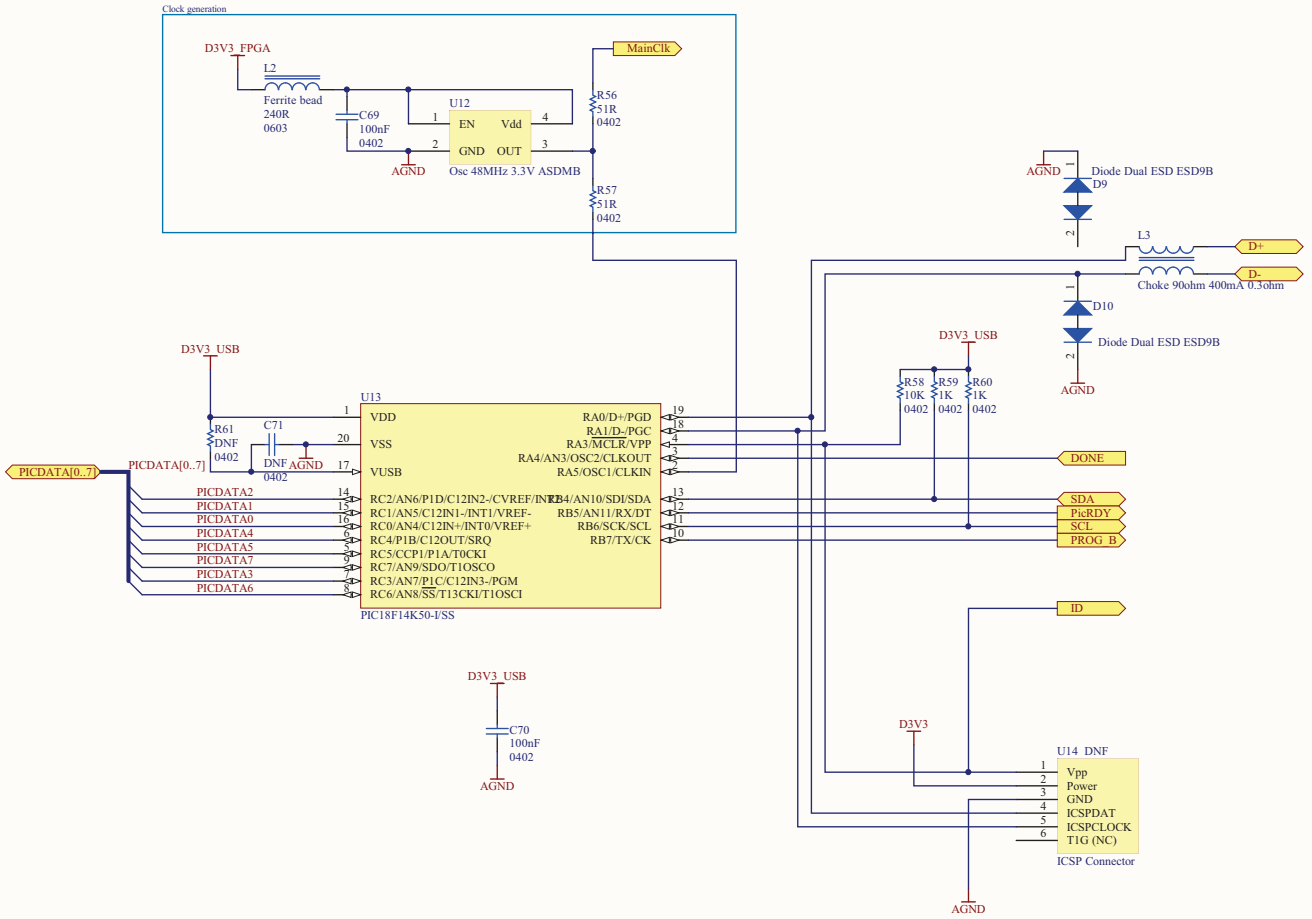

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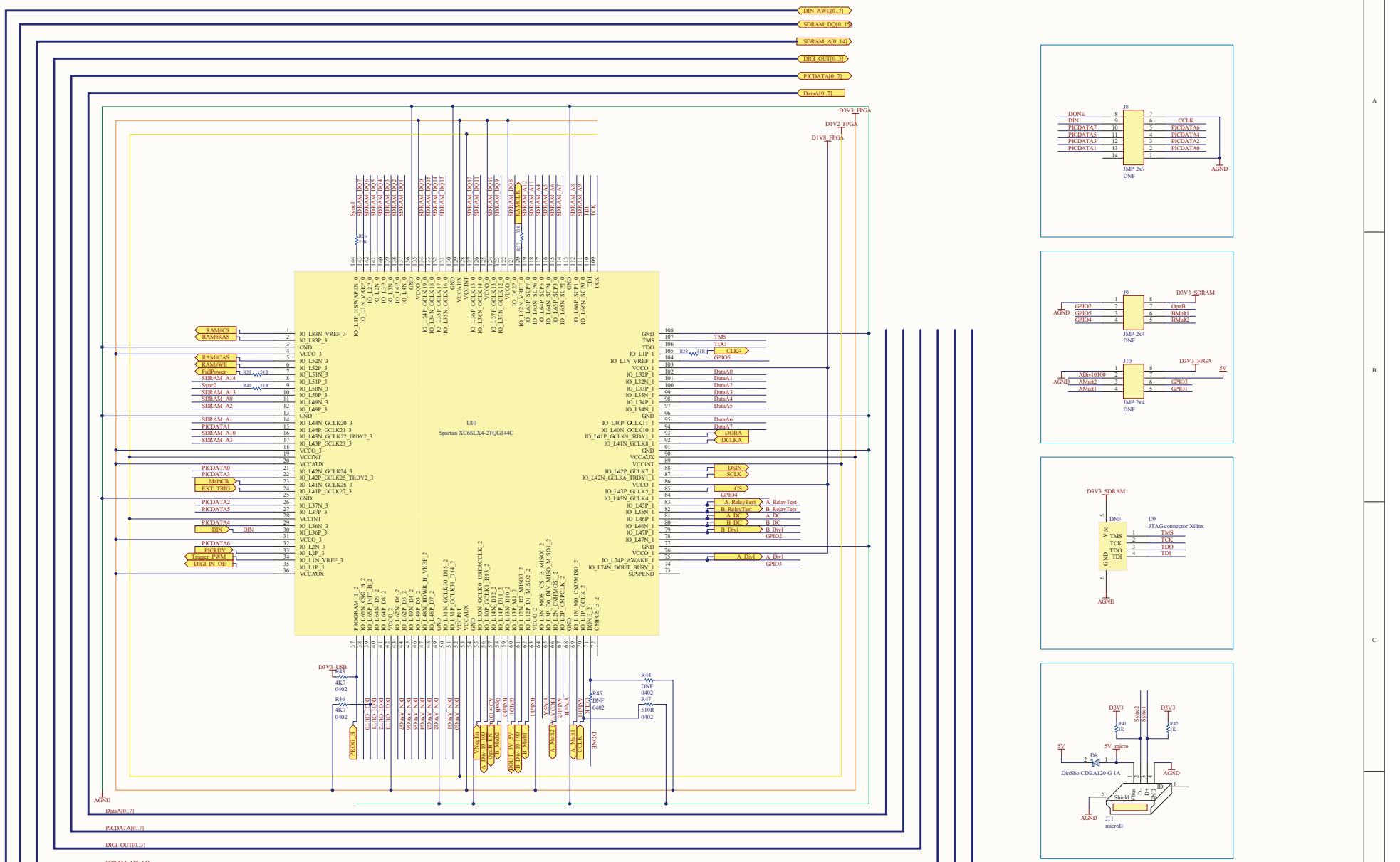

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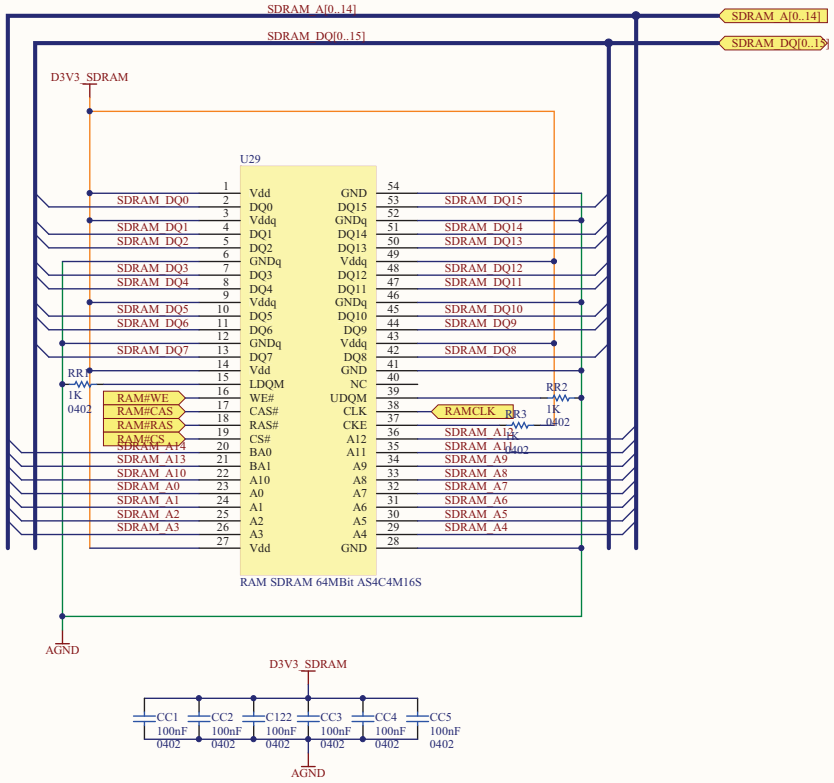

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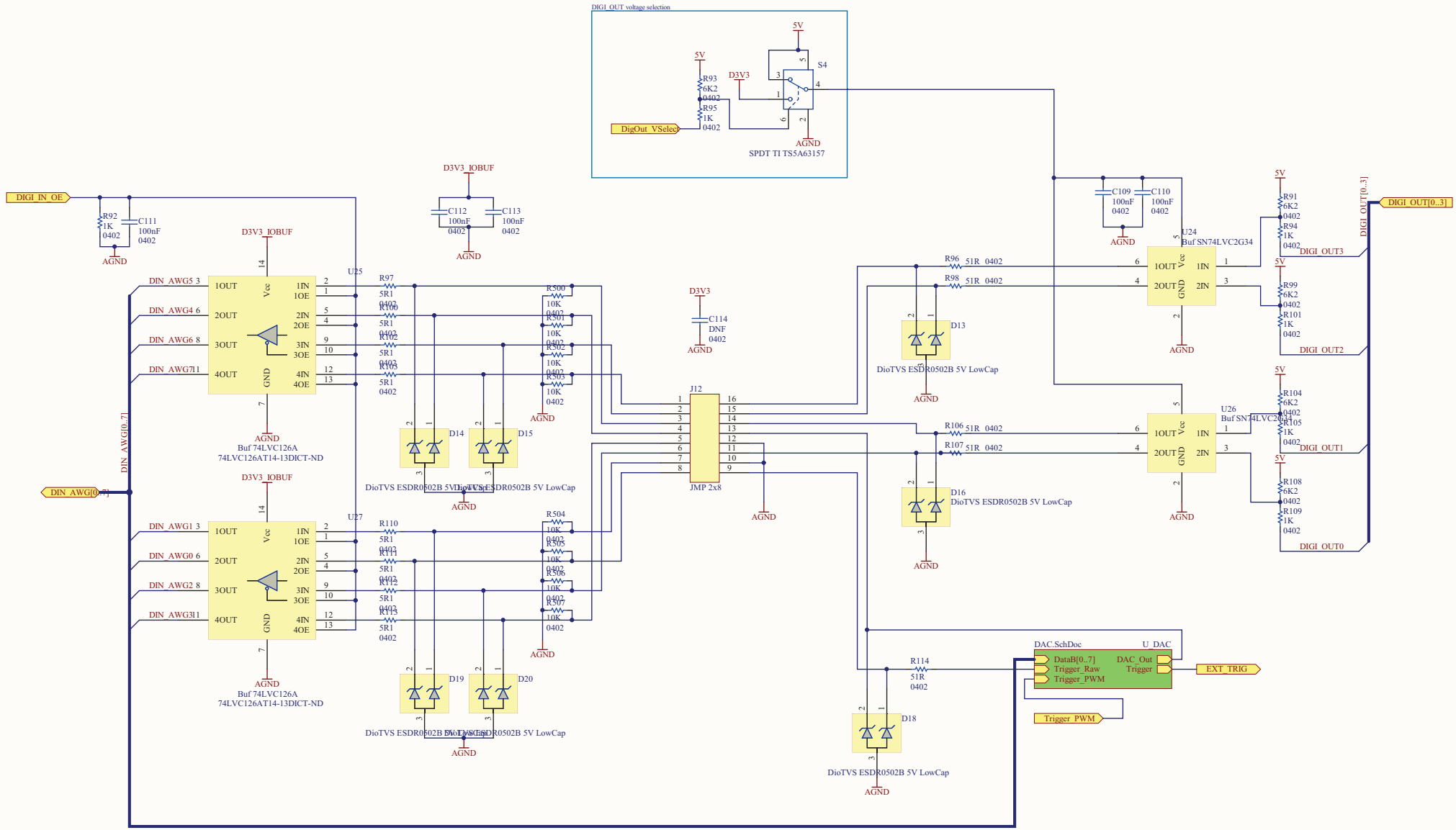

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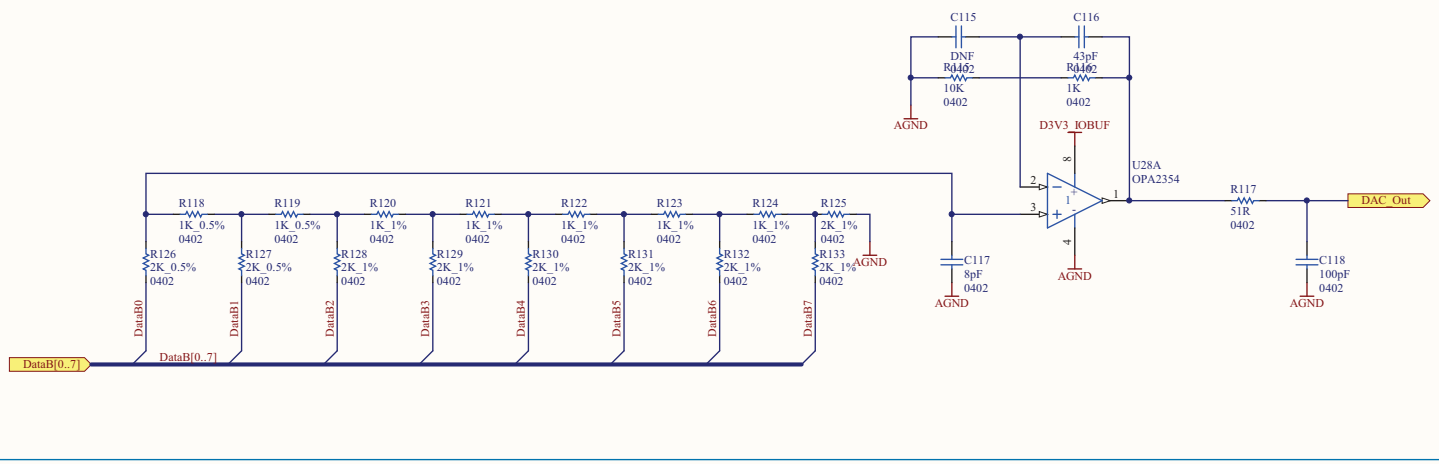
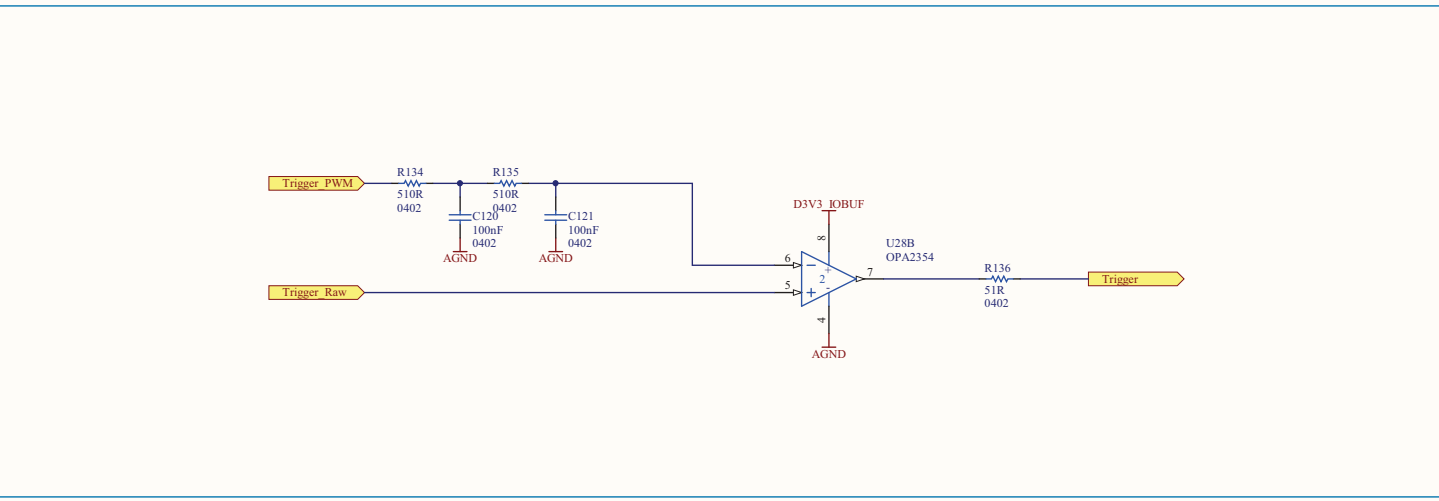
DAC



Comparator



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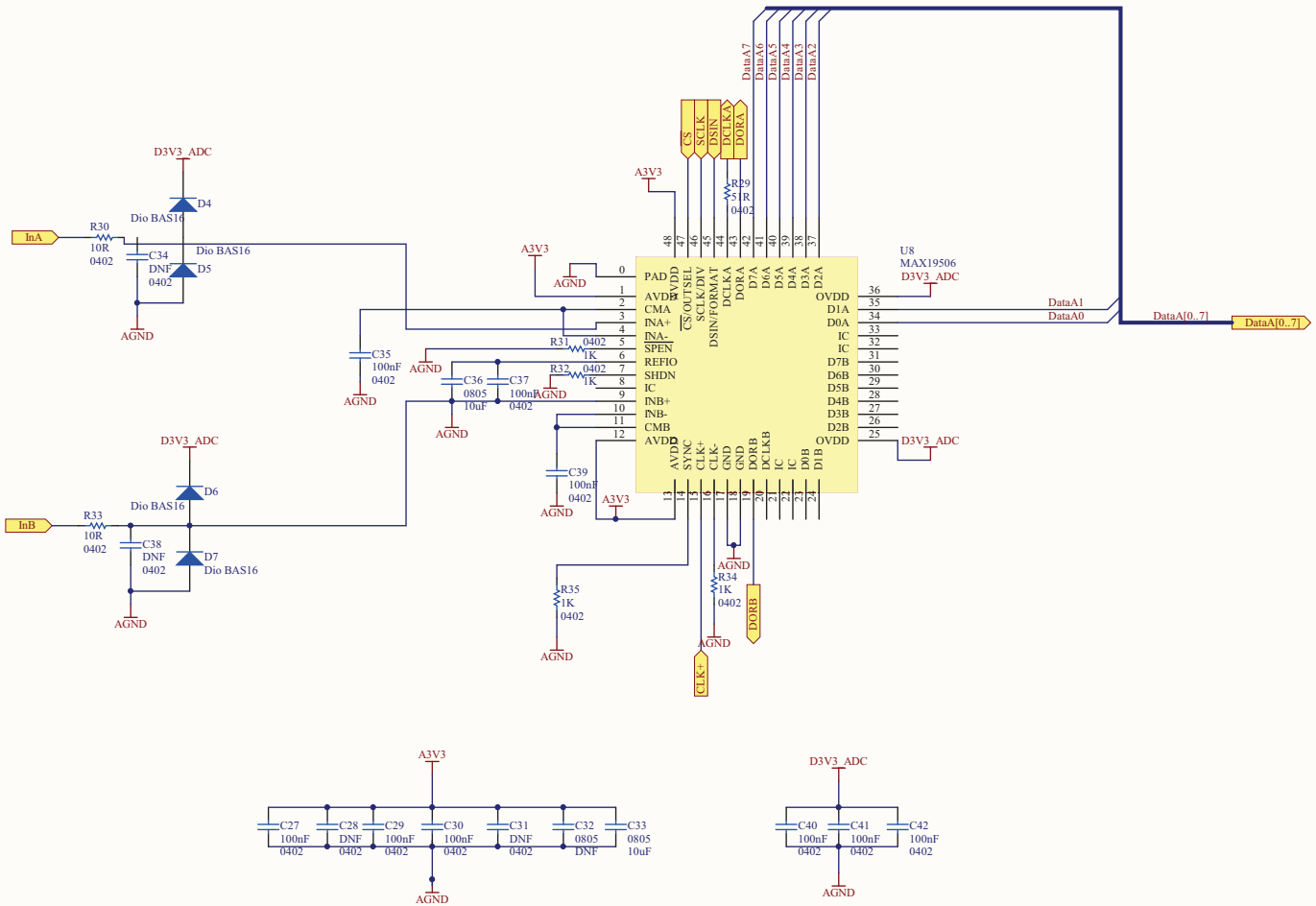

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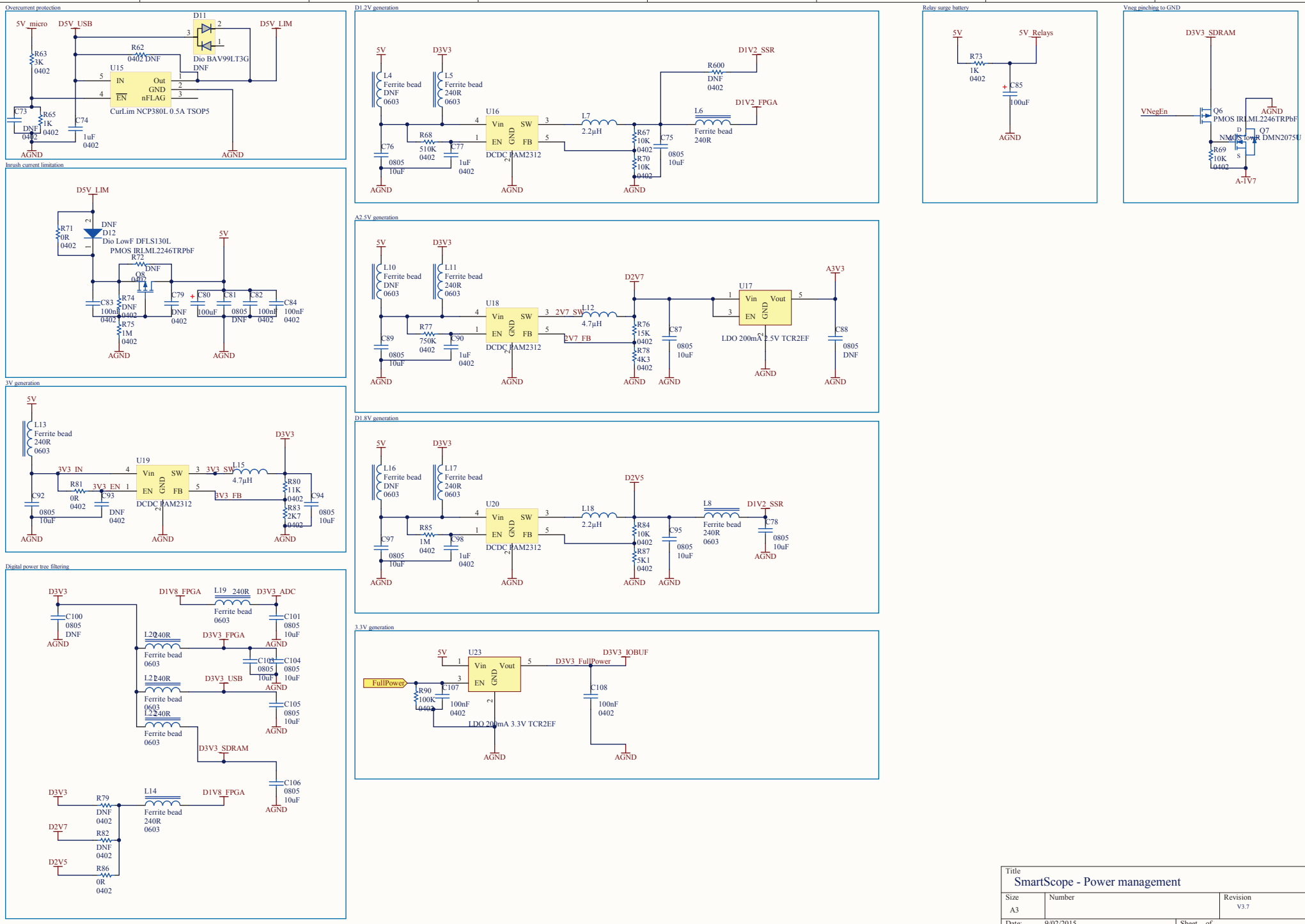

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